Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of generating a signaling pattern for a bus having a plurality of bit lines, said method comprising:

~~for each selected bit line in said plurality of bit lines:~~

selecting a first group of bit lines from a plurality of bit lines to carry a first plurality of signals;

selecting at least one of the remaining bit lines from said first plurality of bit lines not within said first group to carry a second plurality of signals;

generating, using a first linear feedback shift register, [[a]] said first plurality of signals to be sent over said selected first group of bit lines ~~bit line~~; and

further generating, using a second linear feedback shift register,[[a]] said second plurality of signals to be sent over said at least one of the remaining bit lines ~~bit line in said plurality of bit lines other than said selected bit line~~.

2. (original) The method of claim 1, wherein said generating is performed simultaneously with said further generating.

3. (original) The method of claim 1, wherein said first plurality of signals and said second plurality of signals are identical.

4. (original) The method of claim 1, wherein the number of bit lines in said plurality of bit lines is 2^N, where $N \geq 1$.

5. (currently amended) A method of signaling a bus having a plurality of bit lines, said method comprising:

selecting a first group of bit lines from said bus to carry a first plurality of signals;

selecting at least one of the remaining bit lines from said bus not within said first group to carry a second plurality of signals;

transmitting [[a]] said first plurality of signals on ~~a selected one of said plurality~~ said first group of bit lines;

simultaneously transmitting [[a]] said second plurality of signals on ~~one or more of said plurality of bit lines other than said selected bit line~~ said at least one of the remaining bit lines; and

repeating said transmitting and simultaneously transmitting ~~for each bit line in said plurality of bit lines~~.

6. (original) The method of claim 5, wherein said first plurality of signals and said second plurality of signals are identical.

7. (original) The method of claim 5, further comprising shifting said first plurality of signals by at least one bit from said second plurality of signals prior to said repeating.

8. (currently amended) A method of operating a memory connected to a bus, said method comprising:

selecting a first group of bit lines from said bus to carry a first plurality of signals;

selecting at least one of the remaining bit lines from said bus not within said first group to carry a second plurality of signals;

transmitting [[a]] said first plurality of signals on said first group of ~~a selected one of a plurality of~~ bit lines in said bus;

simultaneously transmitting [[a]] said second plurality of signals on said at least one of the remaining bit lines ~~one or more of said plurality of bit lines other than said selected bit line~~; and

performing a data write/read operation at a data storage location in said memory using said bus while said signals in said transmitting and simultaneously transmitting are present on respective bit lines in said bus.

9. (original) The method of claim 8, wherein said performing includes:

performing reading of data as part of said data write/read operation in conjunction with a strobe signal received from a delay locked loop.

10. (original) The method of claim 9, further comprising:

configuring said delay locked loop to provide a delay to said strobe signal so as to enable latching of said data during reading thereof.

11. (original) The method of claim 10, further comprising determining a duration of said delay based on accuracy of said data read during said data write/read operation.

12. (original) The method of claim 11, further comprising repeating said transmitting, simultaneously transmitting, performing and determining ~~for each bit line in said plurality of bit lines~~.

13. (original) The method of 8, further comprising:

changing an operating condition of said memory, wherein said operating condition includes one or more of a supply voltage, a reference voltage, and temperature; and

repeating said transmitting, simultaneously transmitting, and performing with said changed operating condition present.

14. (currently amended) A system comprising:

a memory chip;

a bus having a plurality of bit lines; and

a processor connected to said memory chip via said bus and in communication therewith through said bus, wherein said processor is configured to perform the following:

select a first group of bit lines from said bus to carry a first plurality of data patterns;

select at least one of the remaining bit lines from said bus not within said first group to carry a second plurality of data patterns;

transmit [[a]] said first plurality of data patterns on said first group of bit lines ~~a selected one of said plurality of bit lines in said bus~~, and

transmit [[a]] said second plurality of data patterns on said at least one of the remaining bit lines ~~one or more of said plurality of bit lines other than said selected bit line~~.

15. (original) The system of claim 14, wherein said memory chip includes a plurality of memory cells to store data, and wherein said processor is configured to further perform a data write/read operation at one of said plurality of memory cells using said bus while said first and said second plurality of data patterns are present on respective bit lines in said bus.

16. (original) The system of claim 15, wherein said processor includes a delay locked loop circuit configured to provide a delayed strobe signal during reading of data as part of said data write/read operation, and wherein said processor is configured to adjust a duration of delay for said delayed strobe signal based on accuracy of said data read during said data write/read operation.

17. (original) The system of claim 14, wherein the number of bit lines in said plurality of bit lines is 2^N, where $N \geq 1$.

18. (original) The system of claim 14, wherein said processor is configured to transmit said first plurality of data patterns and said second plurality of data patterns simultaneously.

19. (original) The system of claim 14, wherein said processor includes:

a first linear feedback shift register configured to generate said first plurality of data patterns; and

a second linear feedback shift register configured to generate said second plurality of data patterns.

20. (original) The system of claim 14, wherein said processor further includes a decode circuit having a plurality of output lines, wherein each output line is configured to be connected to one

of said plurality of bit lines so as to allow transmission of said first and said second plurality of bit patterns on respective bit lines.

21. (original) The system of claim 14, wherein said processor is further configured to shift said first plurality of data patterns by at least one bit from said second plurality of data patterns.

22. (original) The system of claim 14, wherein said processor is further configured to perform transmission of said first plurality of data patterns and said second plurality of data patterns for each bit line in said plurality of bit lines.

23. (original) The system of claim 14, wherein said memory chip includes a plurality of memory cells to store data, and wherein said processor is configured to further perform a data write/read operation at one of said plurality of memory cells using said bus after each bit in said first and said second plurality of data patterns is transmitted on respective bit lines in said bus.